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Figure 1 illustrates a two-stage, two-dimensional, multi-processor architecture. The architecture consists of a central processing unit (CPU) connected to a memory unit (MEM) and a network unit (NET). The CPU is connected to the MEM via a bus. The MEM is connected to the NET via a bus. The NET is connected to a network of processors (P1, P2, P3, P4, P5, P6, P7, P8) via a bus. The processors are arranged in a grid and are connected to each other via a network of buses. The diagram is labeled with 'CPU', 'MEM', 'NET', and 'P1' through 'P8'.

1. 本公司之董事、監事、經理及其他重要人員，均應具有適當之專業知識及經驗，並應符合下列條件：

三、联系方式

采 购 人：重庆爱

通讯地址：重庆市

联 系 人：刘先生

联系电话：183015

采购代理机构：重

地 址：重庆市

联系人：王女士

联系电话：173831